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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/632,154	DING, YI
	Examiner	Art Unit
	Khiem D. Nguyen	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 30-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 30-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/02/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 04th, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-17 and 30-38) are pending in the application.

Information Disclosure Statement

The Information Disclosure Statement filed on June 02nd, 2005 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-17 and 30-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (U.S. Patent 6,667,511).

In re claim 1, **Fang** discloses a method for fabricating an integrated circuit comprising a nonvolatile memory comprising a nonvolatile memory cell comprising two

floating gates, a select gate, and two control gates, the nonvolatile memory further comprising a first peripheral transistor, the method comprising:

(a) forming a dielectric layer **108** on a semiconductor substrate **104**, the dielectric layer comprising a first dielectric region **108** ("select gate dielectric'') and a second dielectric region **162** ("first peripheral transistor gate dielectric''), wherein the select gate dielectric **108** and the first peripheral transistor gate dielectric **162** are formed simultaneously (col. 6, lines 10-20 and FIGS. 5c-d);

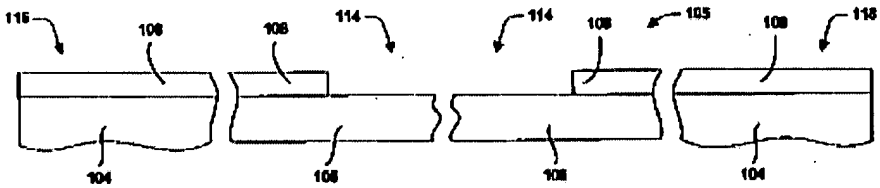

FIGURE 5c

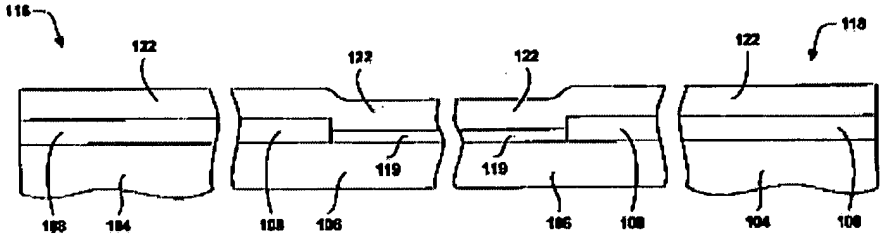

FIGURE 5d

(b) forming a first layer **122** over the dielectric layer and patterning the first layer to provide (i) the select gate on the select gate dielectric **108**, and (ii) a gate **164** for the first peripheral transistor **160** on the first peripheral transistor gate dielectric **162** (col. 6, lines 21-45, col. 7, lines 50-62 and FIG. 5l);

(c) after forming the first layer **122**, forming one or more second layers **144** which provide the floating gates **122b, 122c** and the control gates **144** for the memory cell **180**, the floating and control gates being provided entirely by the one or more second layers, the floating **122b, 122c** and control gates **144** comprising no portion of the first layer **122** (col. 7, lines 31-60 and FIG. 5l).

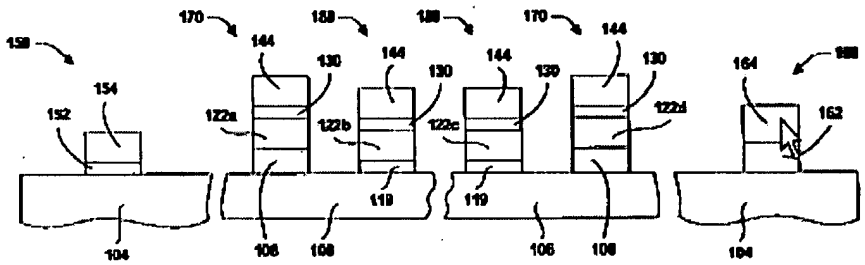

FIGURE 5ℓ

In re claim 2, **Fang** discloses that the memory cell comprises a continuous channel region 106 in the semiconductor substrate **104**, the select gate **122a** controls a conductivity of a portion of the channel region **106**, and each of the floating gates **122b, 122c** overlies a respective other portion of the channel region **106** (col. 6, lines 2-20 and FIG. 5l).

In re claim 3, **Fang** discloses that the control gates **144** overlie the respective floating gates **122b, 122c** (FIG. 5l).

In re claim 4, **Fang** discloses that the one or more second layers 144 are a plurality of layers (FIG. 5l).

In re claim 5, **Fang** discloses that the select gate dielectric **108** and the first peripheral transistor gate dielectric **162** are formed by oxidation of the semiconductor substrate **104** (FIG. 5l).

In re claim 6, **Fang** discloses that the select gate dielectric **108** and the first peripheral transistor gate dielectric **162** comprise silicon oxide (col. 7, lines 31-60).

In re claim 7, **Fang** discloses that the method of Claim 1 further comprising, after forming the first layer **122**, forming a dielectric **130** ("floating gate dielectric") on the semiconductor substrate **104** to separate the floating gates **122b, 122c** from the substrate **104**, wherein the floating gate dielectric **130** is formed of the same material as the select gate dielectric **108** but is thinner than the select gate dielectric 108 (col. 6, line 63 to col. 7, line 2 and FIG. 5l).

In re claim 8, **Fang** discloses that the method of Claim 1 further comprising forming a second peripheral transistor gate dielectric **152** on the semiconductor substrate **104** for a second peripheral transistor **150**, and forming a gate **154** of the second peripheral transistor on the second peripheral transistor gate dielectric **152**, wherein the second peripheral transistor gate dielectric **152** is made from the same material as the select gate dielectric **108** and the first peripheral transistor gate dielectric **162** but the thickness of the second peripheral transistor gate dielectric **152** is different from the thickness of the first peripheral transistor gate dielectric 162 (col. 7, lines 31-60 and FIG. 5l).

In re claim 9, **Fang** discloses that the second peripheral transistor gate dielectric **152** is thinner than the first peripheral transistor gate dielectric **162** (FIG. 5l).

In re claim 10, **Fang** discloses that the select gate dielectric 108 as at least as thick as a gate dielectric **162** of any peripheral transistor **150, 160** in the memory (FIG. 5l).

In re claim 11, **Fang** discloses that the second peripheral transistor gate dielectric **152** is formed after the start of the operation (a) (FIGS. 5a-l).

In re claim 12, **Fang** discloses that the second peripheral transistor gate dielectric **152** is formed before the operation (b) (FIGS. 5a-l).

In re claim 13, **Fang** discloses that the gate **154** of the second peripheral transistor **150** is formed by patterning the first layer **122** in the operation (b) (col. 7, lines 31-60).

In re claim 14, **Fang** discloses that the memory cell **180** is one of a plurality of nonvolatile memory cells of the memory, each memory cell comprising two floating gates **122b, 122c**, a select gate **122a**, and two control gates **144**, wherein: the operation (a) simultaneously forms select gate dielectric **108** for each of the memory cells; and the operation (b) simultaneously forms the select gate **122a** for each of the memory cells on the corresponding select gate dielectric (col. 7, lines 19-60 and FIG. 5l).

In re claim 15, **Fang** discloses that during a memory cell writing operation, the first peripheral transistor **160** is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation (col. 7, lines 31-60).

In re claim 16, **Fang** discloses that during the memory cell writing operation, the first peripheral transistor **160** is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory (col. 7, lines 31-60).

In re claim 17, **Fang** discloses that the memory is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates **122b, 122c** and a channel region **106** of the memory cell, the channel region being located in the semiconductor substrate **104** (FIG. 5l).

In re claim 30, **Fang** discloses that the operation (c) further comprises patterning the one or more second layers **144** to provide the floating **122b, 122c** and control gates **144** (col. 7, lines 31-60 and FIGS. 5a-l).

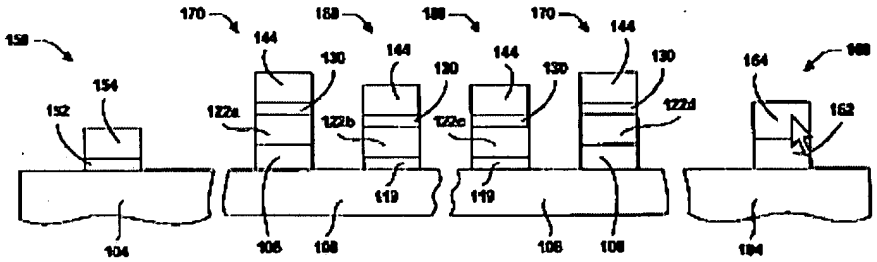

FIGURE 5ℓ

In re claim 31, **Fang** discloses that the first layer patterning comprises:

(b1) patterning the first layer **122** to provide the select gate **122a**; and

(b2) patterning the first layer **122** to provide the gate 164 for the first peripheral transistor **160**;

wherein the operation (c) is performed after the operation (b1) but before the operation (b2) (FIGS. 5a-l).

In re claim 32, **Fang** discloses that the method of Claim 1 further comprising, after forming the first layer **122** but before forming the one or more second layers **144**, forming a dielectric **130** ("floating gate dielectric") on the semiconductor substrate **104** to separate the floating gates **122b, 122c** from the substrate **104** (FIGS. 5a-l).

In re claim 33, **Fang** discloses that the first layer patterning comprises:

(b1) patterning the first layer **122** to provide the select gate **122a**; and

(b2) patterning the first layer **122** to provide the gate **164** for the first peripheral transistor **160**;

wherein the floating gate dielectric **119** is formed after the operation (b1) (FIGS. 5a-l).

In re claim 34, **Fang** discloses that the memory cell **180** comprises a continuous channel region **106** in the semiconductor substrate **104**, and each of the floating gates **122b, 122c** controls a conductivity of a respective portion of the channel region **106** (FIGS. 5a-l).

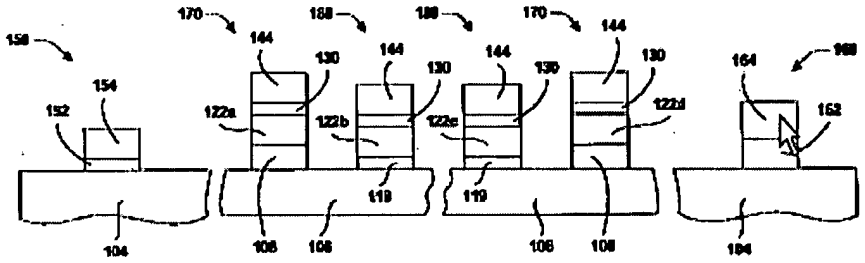

FIGURE 5ℓ

In re claim 35, **Fang** discloses that the select gate controls **144** the conductivity of a portion of the channel region **106** (FIGS. 5a-l).

In re claim 36, **Fang** discloses that the channel's portion **106** whose conductivity is controlled by the select gate **122a** is between the channel's portions **106** whose conductivities are controlled by the floating gates **122b, 122c** (FIGS. 5a-l).

In re claim 37, **Fang** discloses that the memory cell comprises two source/drain regions and a continuous channel region **106** bordering on the source/drain regions, and each floating gate **122b, 122c** of the memory cell overlies a portion of the channel region **106** (FIGS. 5a-l).

In re claim 38, **Fang** discloses that the floating gates **122b, 122c** are adjacent to respective two opposite sidewalls of the select gate **122a** and are insulated from the select gate **122a** (FIGS. 5a-l).

Response to Applicant's Amendment and Argument

Applicant contends that Claim 1 is amended to recite that the floating and control gates are provided entirely by the one or more second layers formed after forming the first layer formed to provide the select gate.

In response to Applicant's contention that Claim 1 is amended to overcome the prior art rejection which recite that "the floating and control gates are provide entirely by the one or more second layers formed after forming the first layer formed to provide the select gate".

Examiner respectfully submits that Applicant's argument is moot in view of the newly discovered reference to Fang (U.S. Patent 6,667,511) applied under 35 U.S.C. 102(e) (See the rejection presented in this Office Action on page 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
July 05th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER